CLAIMS

1. A memory comprising an array of memory cells for storing a plurality of bits, wherein each memory cell is a transistor having two storage regions, each bit of the plurality of bits is stored as complementary charge states in two storage regions, and the two storage regions being from different memory cells.

2. The memory of claim 1 further comprising a sense amplifier having complementary inputs for being coupled to the memory cells having the two storage regions.

3. The memory of claim 2 wherein the sense amplifier is for providing an output at a logic state that is representative of a difference received at the complementary inputs.

4. The memory of claim 2 wherein sense amplifier operates as a comparator of the complementary inputs.

5. The memory of claim 4 wherein the sense amplifier compares current.

6. The memory of claim 4 wherein the sense amplifier compares voltage.

7. The memory of claim 1 wherein each of the two storage regions is further characterized as nanocrystals located between a channel and a control gate of one transistor of a plurality of transistors that comprise the array of memory cells.

8. The memory of claim 7 wherein the nanocrystals comprise silicon.

9. The memory of claim 1 wherein the two storage regions are further characterized as areas of charge storage material located between a channel and a control gate of each of a plurality of transistors that comprise the array of memory cells.

10. The memory of claim 1 further comprising write means for writing a selected bit of the plurality of bits to a first logic state into a selected pair of memory cells by erasing all charge storage regions of all of the memory cells, then programming one of the charge storage regions of one of the selected pair of memory cells.

11. A memory, comprising:

a plurality of memory cells, comprising

a first transistor having a channel region, a control gate, a first current electrode, a first storage region between the channel region and the control gate, and a second storage region between the channel region and the control gate; and

a second transistor having a channel region, a control gate, a first current electrode, a first storage region between the channel region and the control gate, and a second storage region between the channel region and the control gate;

a write circuit, coupled to the first and second transistors, for writing a first logic state by forming a first charge state in the first storage

region of the first transistor and a second charge state, which is different from the first charge state, in the first storage region of the second transistor; and

a sense amplifier having a first input coupled to the first current electrode of the first transistor and a second input coupled to the first current electrode of the second transistor.

12. The memory of claim 11 wherein the sense amplifier is a comparator.

13. The memory of claim 12 wherein the comparator is a current comparator.

14. The memory of claim 12 wherein the comparator is a voltage comparator.

15. The memory of claim 11 wherein the write circuit is further characterized as writing the first charge state to the first storage region of the first transistor by erasing the first storage region and the second storage region of the first transistor and second transistor and writing the second charge state to the first storage region of the second transistor by providing charge to the first storage region of the second transistor.

16. The memory of claim 15 wherein the write circuit is further characterized as writing the first storage region and second storage region of the first transistor and second transistor to the second charge state region prior to erasing the first storage region and second storage region of the first transistor and second transistor.

17. The memory of claim 11 wherein the first storage region and second storage region of the first transistor and second transistor comprise nanocrystals.

18. The memory of claim 11 wherein the first transistor and second transistor are further characterized as having second current electrodes that are coupled to each other.

19. A method of operating a memory having a plurality of bits, comprising:

providing an array of memory cells for the memory, wherein each memory cell comprises a transistor having two storage regions;

erasing the two storage regions of the memory cells;

selecting a first memory cell and a second memory cell of the array of memory cells for programming a first bit of the plurality of bits of the memory;

programming the first bit by writing a first storage region of the two storage regions of a first transistor while keeping a first storage region of the two storage regions of a second transistor erased;

generating a first signal that is representative of charge stored in first storage region of the first transistor, and a second signal that is representative of charge stored in the first storage region of the second transistor; and

comparing the first signal to the second signal to determine a logic state of the first bit.

20. The method of claim 19 further comprising implementing the two storage regions of the first transistor and the second transistor with nanocrystals of silicon.

21. The method of claim 19 wherein the two storage regions of the first transistor and the second transistor comprise storage material capable of storing charge between a channel and a control electrode of each of the first transistor and the second transistor.

22. The method of claim 19 wherein the comparing is achieved by comparing current.

23. The method of claim 19 wherein the comparing is achieved by comparing voltage.

24. A method of operating a memory having a plurality of bits, comprising:

providing an array of memory cells for the memory, wherein each memory cell comprises a transistor having a first storage region and a second storage region between a channel and a control gate;

generating a first signal that is representative of charge stored in the first storage region of a first transistor, and a second signal that is representative of charge stored in the first storage region of a second transistor; and

comparing the first signal to the second signal to determine a logic state of a first bit of the plurality of bits.

25. A method of operating a memory having a plurality of bits, comprising:

providing an array of transistors, wherein each transistor has a first storage region and a second storage region;

comparing charge stored in the first storage region of a first transistor to charge stored in the first storage region of a second transistor to determine a logic state of a first bit of the plurality of bits; and

comparing charge stored in the first storage region of a third transistor to charge stored in the first storage region of a fourth transistor to determine a logic state of a second bit of the plurality of bits.

26. The method of claim 25 further comprising implementing the first storage region and the second storage region with nanocrystals.

27. The method of claim 25 further comprising implementing the first storage region and the second storage region with a storage material capable of storing charge between a channel and a control electrode of each transistor.

28. The method of claim 25 wherein the comparing charge stored in the first storage region of a first transistor to charge stored in the first storage region of a second transistor further comprises:

generating a first signal that is representative of charge stored in the first storage region of the first transistor, and generating a second signal that is representative of charge stored in the first storage region of the second transistor; and

comparing the first signal to the second signal to determine the logic state of the first bit.

29. The method of claim 28 wherein the comparing the first signal to the second signal is achieved by comparing voltage.

30. The method of claim 28 wherein the comparing the first signal to the second signal is achieved by comparing current.